A 12-Channel Bidirectional Neural Interface Chip with Integrated Channel-level Feature Extraction and PID Controller for Closed-loop Operation

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***Abstract*—This paper presents a bidirectional neural interface, consisting of 12-channel low-noise amplifiers, channel-level neural feature extraction and proportional-integral-derivative (PID) controller, voltage and current mode analog-to-digital converters (ADC), and 12-channel multi-mode stimulators. The neural amplifier features a wide-band from 0.5Hz to 10kHz with a noise floor of 3.02μVrms. The input stage has been designed for high stimulation voltage tolerance, and fast stimulation artifact recovery. The digitally assisted, analog parallel feature extraction processor features an ultra low power consumption while performing 1) neural signal energy extraction in programmable frequency band and time window, or 2) action potential detection using a current-mode time-amplitude window discriminator. A programmable PID controller has been implemented at the channel-level for closed-loop operation. A 640nW 8-bit current-mode ADC featuring a FoM of 10.7fJ/conv-step at a sampling rate of 250kSps has been designed for action potential digitization, and a voltage-mode SAR ADC with a ENOB of 9.1 and FoM of 34.2fJ/conv-step has been implemented for neural features and local field potential digitizations. The multi-mode stimulator can be programmed to perform monopolar or bipolar, symmetrical or asymmetrical charge balanced stimulation with a maximum current of 4mA and a compliance voltage up to +/-5V in arbitrary channel configuration. The chip has been fabricated in 0.18μm HV-CMOS technology, occupying a silicon area of 2.2 mm^2. The whole chip dissipates 276μW on average. Bench testing, in-vitro and in-vivo experimental results are presented in this paper.**

I. Introduction

Closed-loop activity-dependent neural stimulation has been widely used in the study of brain activities [1]. Traditional approaches uses high-speed external computer to perform the signal processing, which impractical due to the need for a massive computations for a multiple electrode array (MEA). In addition, the power consumption of the system increases greatly for real-time signal processing. Recently, low-power, multipe channel, brain-machine-interface systems with on-chip signal processing have been reported in the literature [3–5]. In these applications, neural features, i.e., action potential and/or local field potential are widely used as an effective feedback indicators for the control of the stimulation parameters. Both analog and digital implementations of the neural feature extraction modules have been reported. Analog implementation features a higher processing efficiency, but suffers from poor programmability and linearity. While the digital makes use of a serial processor, which won't be able to provide an efficient feature extraction capability for large number of channels.

In this work, we proposed a reprogrammable, bidirectional neural interface system with an integrated digitally assisted, analog parallel feature extraction units and closed-loop controller. The ultra low-power, low-bandwidth analog parallel processing unit features a high energy efficiency over high bandwidth serial digital signal processing. Fig. 1 illustrates an application of a general-purpose wireless closed-loop brain machine system using the proposed chip. The proposed chip performs a noise sensitive, neural signal acquisition, a high safety neural stimulation, and a computationally intensive feature extraction. At the same time, the system takes advantage of the programmability of general purpose microcontrollers with on-chip flash memory, and low-power universal wireless protocols (Bluetooth, Zigbee, etc.) to interface with computers or work stations.

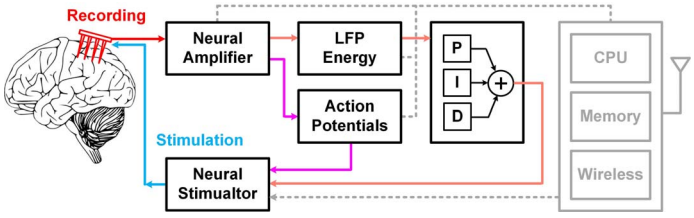

Fig. 1. A miniature brain machine interface system using the proposed bidirectional neural interface with on-chip neural feature extraction and PID controller for closed-loop operation.

This paper is organized as follows. The Section II describes the design of each individual modules. Experimental results are shown in Section III, while Section IV concludes the entire work.

II. Circuits Implementation

Fig. 2 shows the system architecture of the bidirectional neural interface chip. The system consists of 1) a 12-channel analog front-end with low-noise amplifier, feature extraction units and PID controller, 2) two ADCs with different specifications, 3) 12-channel multi-mode stimulators, and 4) peripheral modules including power, reference and communication circuits. The analog front-end and voltage mode ADC are designed to operate at 1.8V. The current mode ADC and digital circuits operate at 0.9V. The stimulator back-end is designed in 5.5V for high compliance voltage. The analog references are generated on-chip, while the digital clock is provided by the external low-power wireless microcontroller.

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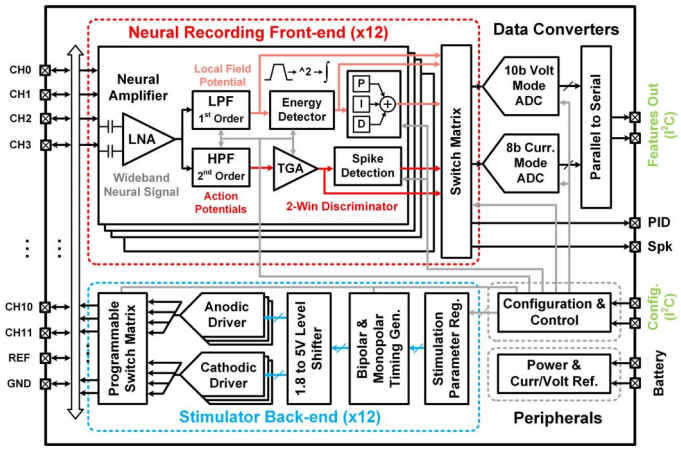

Fig. 2. System architecture of the proposed bidirectional neural chip.

A. Recording Front-end

In the proposed analog front-end, wide-band neural signals are acquired by low-noise neural amplifiers, and then filtered into local field potential (LFP) and action potential (AP) bands, separately. The energy feature of the LFP is extracted in a filter with programmable passband and window length. The action potential is detected by a discriminator with two time-amplitude windows. A programmable PID controller is integrated at the channel-level to realize the close-loop control by the extracted features.

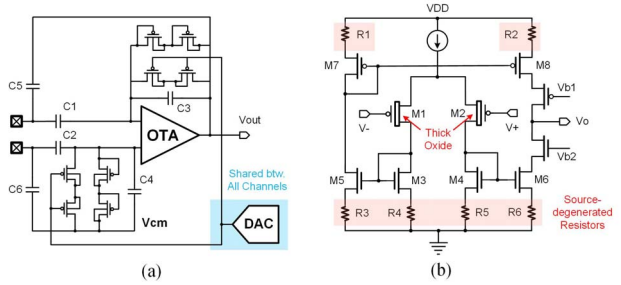

Fig. 3. Circuits schematic of the neural amplifier. (a) Capacitor coupled neural amplifier with pole shifting for stimulation artifact suppression. (b) OTA design with source degeneration current mirror.

The circuits schematics of the proposed neural amplifier is shown in Fig. 3. Weak-inversion transistors are used to tune the feedback resistance, so that the highpass pole can be shifted into higher frequency for fast recovery from stimulation artifacts. Positive current feedback is used to boost the input impedance [7]. Source degeneration current mirrors are used in the OTA to lower the noise contribution from the current mirror, thus the total noise can be optimized without sacrificing the phase margin. Thick oxide transistors are used in the input differential pair to prevent high voltage damage.

Given the low frequency nature of the neural signal, very large time constant has to be implemented on chip. g_mC block is chosen in this work since it has high tunability and small area compared to an op-amp based filter, at the same time, it doesn't require various clock generation circuits that is the case for switched capacitor based filter. An area-efficient digital programmable g_m block is proposed, as shown in Fig. 4. Diode connected feedback transistors are used to extend the linear input range, and a 6-bit W-2W current steering DAC is integrated to tune the g_m.

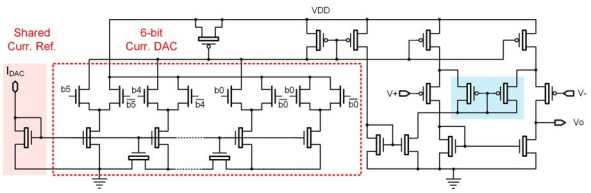

Fig. 4. The proposed digital programmable g_m block with compact 6 bit W-2W current steering DAC.

The LFP energy detection circuits are shown in Fig. 5 (a). The LFP signal is first band passed in the frequency range of interest, squared to get the energy, and then integrated in a programmable time window. A staggered tuned 4th order band-pass filter is used. The center frequency and quality factor of each biquad are independently tuneable. The g_m blocks are set to be g_{m1}=g_{m2}, and g_{m3}=g_{m4}. DAC references are shared to save area. Only two grounded capacitor with same size C_1=C_2 are used in each biquad. Compared with prior publications, this implementation features small area, high digital programmability and ultra low power. The transfer function of the given bandpass filter is given by:

$$H(s) = \frac{sg_{m1}/C_1}{s^2 + sg_{m2}/C_1 + (g_{m3}g_{m4})/(C_1C_2)} \quad (1)$$

$$\omega_C = \sqrt{(g_{m1}g_{m2})/(C_1C_2)} = g_{m1}/C_1 \quad (2)$$

$$Q = \sqrt{(C_1g_{m3}g_{m4})/(C_2g_{m2}^2)} = g_{m3}/g_{m1} \quad (3)$$

The proposed g_mC based PID controller is shown in Fig. 5 (b). The gains for each of the P, I, and D components are independently programmable. The transfer function of the PID controller is:

$$\frac{V_{OUT}(s)}{V_{ERR}(s)} = \frac{g_{m1}}{g_{m6}} + \frac{g_{m2}}{sC_1 + g_{m2}}\frac{g_{m3}}{g_{m6}} + \frac{sC_2}{sC_2 + g_{m4}}\frac{g_{m5}}{g_{m6}} \quad (4)$$

where V_{ERR}=V_{REF}-V_{IN}. The gain of the P, I and D components are Kp=g_{m1}/g_{m6}, Ki=g_{m3}/g_{m6}, and Kd=g_{m5}/g_{m6}. A Gilbert multiplier and a lossy integrator has been used for energy detection and integeration [8].

A current-mode action potential detection unit has been integrated in each channel. Two amplitude thresholds and a time window are used to discriminate the action potentials from different neurons, as illustrated in Fig. 6 (a). The signal voltage is first converted to current with a tunable transconductance, and then compared with the two threshold currents during the depolarization and repolarization processes in a programmable interval time window. The threshold currents and window length can be set independently for each channel.

B. Analog to Digital Converters

Two ADCs have been integrated on-chip to optimize the power efficiency of the data conversion. An 8-bit low-power current mode ADC has been implemented for the conversion of high bandwidth action potential signals. Current signals

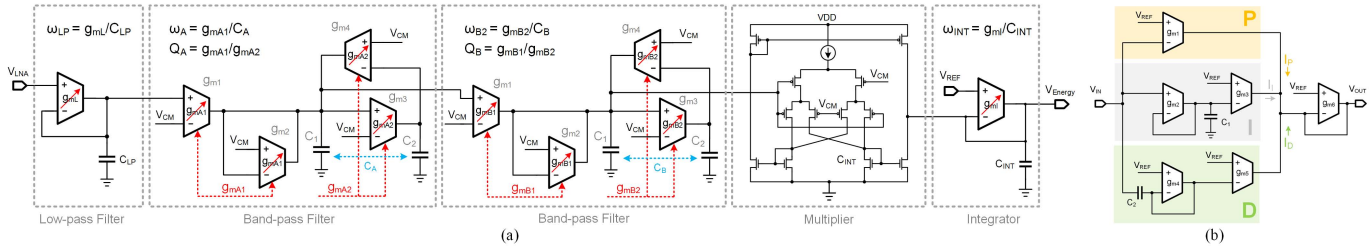

Fig. 5. (a) The processing circuits of the local field potential signal. The center frequency and the quality factor of the two-stage staggerred biquad bandpass filter can be independently programmed. (b) The circuits implementation of the proposed programmable PID controller.

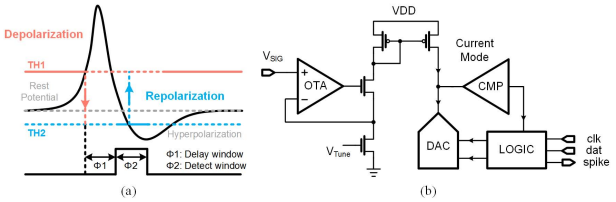

Fig. 6. (a) Illustration of the action potential detection principle. (b) circuit schematic of the programmable current mode spike detection uint with integrated programmable window-discriminator.

are more robust to noise in routing lines while the current mode operation allows lower supply voltage for high dynamic range data conversion. A 10-bit voltage mode SAR ADC with an energy efficient monotonic capacitor switching procedure [6] has been integrated. Single-ended operation is used in the feature extraction to reduce the area; this requires a single to differential converter in the ADC to drive the differential sampling capacitor array. Power-gating has been used to shut down the ADC modules to minimize the power leakage.

C. Multi-mode Stimulator

A 12-channel multi-mode neural stimulator is also introduced in this work. The stimulator can perform monopolar or bipolar, symmetrical or asymmetrical charge balanced stimulation with programmable amplitude, pulse width, and channel configuration. Three stimulating current drivers with high output impedance are integrated to provide up to three channel of simultaneous stimulation. A 6-bit current DAC is integrated in each driver to generate the current reference. In the low current mode, the output is 4μA to 250μA. In the high current mode, the output is 64μA to 4mA. High driving voltage and thick oxide MOSFETs are used to provide enough compliance voltage for high impedance electrodes. A novel high-voltage switch matrix is proposed, as shown in Fig. 7 (a). The proposed switch matrix minimizes the routing and the overall area of the stimulator. The simulation topology and the corresponding timing are shown in Fig. 7 (b) and (c), respectively.

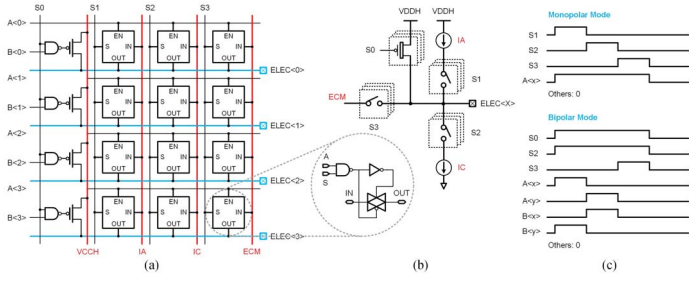

Fig. 7. The proposed multi-mode stimulator can be programmed as monopolar or bipolar, symmetrical or asymmetrical mode in arbitrary channel configuration. (a) High density switch matrix. (b) Stimulation topology. (c) Timing of monopolar and bipolar modes.

III. Experimental Results

The design has been fabricated in 180nm HV CMOS process, occupying a silicon area of 4.5mm×1.5mm. The proposed system and the die photo are shown in Fig. 8. The measured performance of the system is listed in Table I.

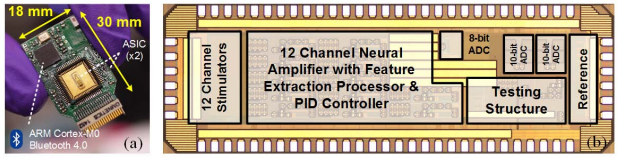

Fig. 8. (a) A wireless portable Brain machine brain interface (BMBI) system integrated the proposed chip. (b) Die photo of the fabricated chip with major blocks highlighted.

TABLE I
Specifications Summary

Analog Front-end		**ADC (Volt Mode/CurrMode)**	
LNA Gain	40dB	Sampling Rate	1MSps/250KSps
LNA Bandwidth	0.5 - 10kHz	ENOB	9.1/7.9
LNA Noise	3.02uV	FoM(fJ/step)	34.2/10.7
NEF	3.72	**Stimulator**	
Energy Extraction		Max. Stim. Current	4mA or 250uA
3dB filter	100 - 5kHz	Amplitude Res.	6-bit
Stagger tuning	1Hz - 200Hz	Pulse width	1us - 250us
Quality Factor	0.5 - 32	**Power**	
Window length	10 - 500ms	LNA + PGA	20uW per Ch.
Action Potential Discriminator		Energy Detection + PID	1uW per Ch.
Thresholds	6-bit	Stimulator (standby)	2uW
Latency	10us	Total (avg.)	276uW (12 Ch.)

The measured input referred noise of the analog front-end is 3.02μVrms in a 10kHz bandwidth. The measured frequency response of the bandpass filter is shown in Fig. 9, where (a) shows the tuning of the center frequency, and (b) shows the tuning of the quality factor. Fig. 9 (c) shows the frequency response the 4th-order stagger tuned filter when programmed for the three neural signal frequency bands (α: 8-12 Hz, β: 15-30 Hz, and γ 30-100 Hz). The measured transient response of a biquad stage is shown in Fig. 10 (a), where the input signal is a constant amplitude sine wave sweeping from 0.1Hz to 1kHz. Fig. 10 (b) shows the measured output of the Gilbert multiplier used for squaring the signal. Fig. 10 (c) shows the measured output of the energy integration circuits with

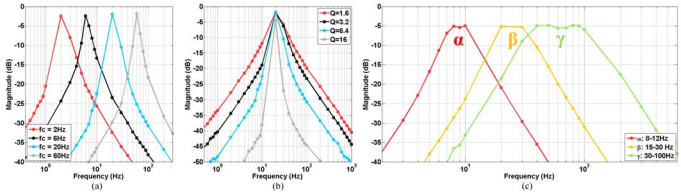

Fig. 9. Measured frequency response of the bandpass filter. (a) tuning of the center frequency of one biquad. (b) Tuning of the quality factor of one biquad. (c) Stagger filter tuned to α, β and γ band.

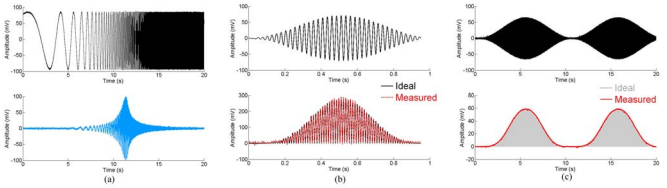

Fig. 10. (a) Measured response of one biquad filter with a input sine wave frequency sweeping from 0.1Hz to 1kHz. (b) Measured output of the Gilbert Multiplier with a amplitude modulated 40Hz signal. (c) Measured output of the LFP energy detection circuits.

an amplitude modulated 40Hz sine wave as input. The PID controller's performance is evaluated with a system of RC ladder network. The measured output in different P, I, and D parameters configuration are shown in Fig. 11 (a). The output of the RC ladder network is fed back to the PID controller and compared with a pre-set reference signal to find the error signal. The design proves to be programmable over a large range, and useful in versatile closed-loop applications. The spike detection circuits are tested with synthesized action potential signals. The detected spike is used to trigger a pre-defined stimulation pulse train. The stimulation is tested in-vitro using 75μm tungsten electrode and 0.9/100mil Sodium Chloride, as shown in Fig. 11 (b).

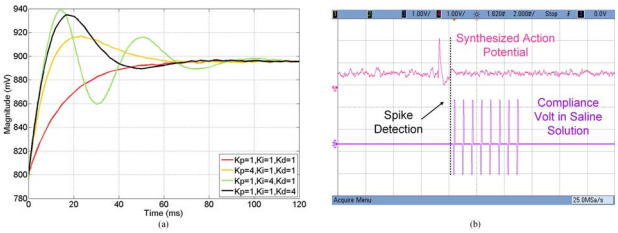

Fig. 11. (a) Measured transient response of the PID controller circuits tuning the parameters. (b) Measured the action potential triggered stimulation in Sodium Chloride.

In vivo testing of the device was conducted in a male rhesus macaque (Macaca mulatta) with electrodes implanted chronically in the left hippocampus. A battery powered system consisting of two of the designed chips and a low-power ARM Cortex M0 based 2.4GHz wireless microcontroller has been integrated. The size of the system is 30 mm$\times$18 mm, and the weight is 15g including the battery. Hippocampal field potentials were recorded over a 17-h period while the animal was freely behaving in his home cage. The extracted energy in β band (15-30Hz) as well as power spectrum of the entire sampling procedure is plotted in Fig. 12.

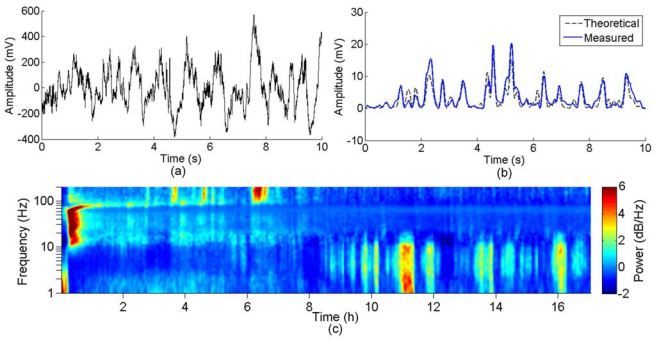

Fig. 12. In-Vivo LFP recording (top) and the extracted energy in beta band (15-30Hz) compared with the theoretical computation (middle). The bottom is power spectrum of the 17-h period.

TABLE II
COMPARISON WITH BIDIRECTIONAL NEURAL INTERFACE CHIP

	[3]	[4]	[5]	This work
Rec/stim Ch. #	4/8	32/16	1/1	12/12
AFE Noise	6.3μVrms	100nV/rtHz	3.42μVrms	3.02μVrms
Bandwidth	0.64-6kHz	0.5-1.7kHz	0.1-12.3kHz	0.5-10kHz
ADC ENOB	5.6 (log)	12	10	9.1/7.9
Feature Ext.	Serial DSP	Serial DSP	Serial DSP	Parallel analog
Feedback controller	global PI	NA	NA	channel PID
Stim. mode	monopolar	monopolar	monopolar	mono&bipolar
Stim. artifact rej.	LFP	LFP	Subtraction	Pole shifting
CMOS Technology	0.18um	0.25um HV & 90nm	0.35um	0.18um HV

IV. CONCLUSION

In this paper, a 12-channel bidirectional neural interface chip has been reported. The proposed design features a multiple channel ultra low-power analog feature extraction and closed-loop controller. The system is highly programmable and energy efficient. A comparison with recent reported designs of bidirectional neural interface is listed in Table II. The proposed system provides a promising solution for brain machine interface applications, especially for closed-loop operations.

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